Anadi Goyal

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Research Interests

Efficient and accelerator-aware AI inference | hardware acceleration of deep learning models | adversarial robustness and AI security.

EDUCATION

Indian Institute of Technology Jodhpur **Dec 2021-June 2025**
Bachelor of Technology in Mechanical Engineering *GPA-7.81*

Surbhi Senior Secondary School **2020**
Rajasthan Board of Secondary Education (R.B.S.E) *Percentage: 89.6%*

Publications

1. Nandish Chattopadhyay, Anadi Goyal, Anupam Chattopadhyay, and Chandan Karfa. *"STRAP-ViT: Segregated Tokens with Randomized-Transformations for Defense against Adversarial Patches in ViTs"* **Design Automation Conference (DAC), 2026 (Accepted).**
2. Anadi Goyal, Nandish Chattopadhyay, Anupam Chattopadhyay, and Chandan Karfa. *"Adversarial Efficiency Degradation for Vision Transformer by Exploiting Input-adaptive Optimization: A Survey."* **Artificial Intelligence and Internet of Things (AIIoT), 2025 (Accepted).**
3. Anadi Goyal, Gaurav Sangwan, Aradhya Patel, and Palash Das. *"HAVIT: An Efficient Hardware-Accelerator for Vision Transformer with Informative Patch Selection Techniques."* **ACM Transactions on Architecture and Code Optimization (ACM TACO), 2025 (Accepted). [Paper]**
4. Satyaswaroop Nayak, Anadi Goyal, Sheel Sindhu Manohar, Dip Sankar Banerjee, and Palash Das, *"Enhanced Prefetching via Dynamic Multi-Step SARSA based Reinforcement Learning."* **IEEE Embedded Systems Letters (ESL), 2025 (Accepted). [Paper]**
5. Akshansh Yadav*, Anadi Goyal* and Palash Das, *"Hybrid Token Selector based Accelerator for ViTs."* **Design, Automation and Test in Europe (DATE), IEEE, 2025. [Paper, Presentation]**
6. Deepraj Majumdar, Anadi Goyal, Sparsh Mittal, Shirshendu Das, and Palash Das. *"Secure Hardware Accelerator for Resilience Against Adversarial Attacks in ViTs."* **IEEE Transactions on Computers (TC) — Under Review, Final Round.**

*both authors contributed equally to this work

Work Experience

Research Assistant *July 2025 – present*
Department of Computer Science & Engineering, Indian Institute of Technology Guwahati
Supervisor: Dr. Chandan Karfa, IIT Guwahati and Dr. Anupam Chattopadhyay, NTU Singapore

- **Key Contributions:**
  - Developed model-agnostic defenses for adversarial patch attacks on Vision Transformers.
  - Analyzed efficiency-targeted adversarial attacks exploiting optimization strategies in ViTs.
  - Proposed approaches to enhance robustness of optimized/accelerated ViT inference pipelines.
  - Investigating stronger energy-based attacks on efficient AI inference hardware.
  - Improving robustness of large language models against jailbreak prompts.
- **Outcome: Manuscripts accepted in DAC'26 and AIIoT'25.**

Research Projects

Hardware-Software Co-Design for Optimized Inference of Computer Vision Models *Jan 2023 - Sept 2024*
Supervisor: Dr. Palash Das, IIT Jodhpur

1. **Hardware Acceleration of Vision Transformers Using Informative Patch Selection.**

- **Key Contributions:**
  - Proposed lightweight and image-adaptive **informative patch selection techniques** to achieve efficient yet accurate Vision Transformer (ViT) acceleration.
  - Designed and implemented **dedicated hardware (ASIC)**, HAVIT, specifically to accelerate both the proposed informative patch selection algorithms and the Vision Transformer (ViT) algorithm.
- **Outcome:** Achieved significant improvements in acceleration efficiency and accuracy; **accepted in ACM Transactions on Architecture and Code Optimization (ACM TACO), 2025** .

2. **Accelerating Vision Transformers with a Hybrid Token Selection Approach on FPGAs.**
   - **Key Contributions:**
     - Analyzed **token selector placement** in the ViT architecture, optimizing accuracy and computational trade-offs in attention-based methods.
     - Proposed a **feature-based token pruning strategy** for early layers, reducing reliance on attention scores for single-stage pruning.
     - Improved the multi-stage token pruning process by introducing a **hybrid methodology,** reducing execution time between 29-40% with minimal accuracy loss.
     - Designed and implemented a hardware accelerator for the ViT backbone and the proposed token selection method on **FPGA** using **Vitis HLS and Vivado**.
   - **Outcome:** Achieved significant improvements in performance and efficiency; **accepted as a regular paper in DATE conference 2025.**

Secure Hardware Accelerator for Resilience Against Adversarial Attacks in ViTs *May 2024 - July 2025*
Supervisor: Dr. Palash Das, IIT Jodhpur
- **Key Contributions:**
  - Developing a **lightweight rectifier** algorithm to eliminate adversarial noise.
  - Implementing a **custom hardware accelerator on FPGA** for real-time rectification.
  - **Evaluating** system performance under various attack scenarios (**white-box, black-box**).
- **Outcome:** Increased resilience of ViTs while maintaining low overhead; **manuscript under finals rounds of review in IEEE Transactions on Computer (TC).**

Reinforcement learning based Prefetcher Design *May 2024 - May 2025*
Supervisors: Dr. Dip Sankar Banerjee and Dr. Palash Das, IIT Jodhpur
- **Key Contributions:**
  - Modified existing RL-based Q-value updation process to improve cache coverage and reduce cache pollution.
  - Developed a hardware to estimate the area and power overhead of the prefetcher.
- **Outcome:** Manuscript published in a IEEE Embedded Systems Letters (ESL).

Application Project

Efficient Disease Prediction Using Blood Samples with Vision AI Models *Aug 2024- Dec 2024*
Supervisors: Dr. Hirshikesh and Dr. Palash Das, IIT Jodhpur
- **Key Contributions:**
  - Fine-tuning a Vision Transformer (ViT) on blood sample images for accurate detection of diseases based on specific blood-related features within images of blood samples.
  - Developing a custom hardware accelerator for accelerating the algorithm and implementing it on an FPGA.

Teaching Experience

Indian Institute of Technology Jodhpur *Fall 2023 & 2024*
Teaching Assistant for Python for Data Engineering Course under Dr. Palash Das and Dr. Bikash Santra.
- Set up Python assignments, organized lab sessions, and evaluated the students enrolled in the course.
- Closely guided and mentored a group of 30 students in the course, holding periodic discussions and feedback sessions.

Skills & Achievements

- **Programming Languages:** C, C++, Python, HTML+CSS.
- **Tools:** Xilinx Vivado, Xilinx Vitis HLS, Latex.
- **Technologies:** Pytorch, tensorflow, Pynq, qiskit.
- Awarded **fellowship** to attend **VLSID 2025.**
- Received a **grant of INR 130,000 ($1500) from IEEE CEDA** to present research at DATE 2025, France.